IN THE CLAIMS:

Claims 1-47 (Canceled)

48. (Previously Presented) An integrated circuit device comprising:

a metallization interconnect system overlying a semiconductor substrate, the metallization interconnect system including at least a first and a second interconnect feature located within a dielectric layer;

a power bus located over the metallization interconnect system, the power bus comprising an alloy of aluminum and copper, and further wherein the power bus includes a first contact pad region configured for connection external to the integrated circuit device that is in contact with the first interconnect feature, and a second region in contact with the second interconnect feature; and

a passivation layer overlying at least a portion of the power bus to expose at least a portion of the first contact pad region and protect the second region.

49. (Previously Presented) The integrated circuit device of claim 48 wherein a plane of an upper surface of the first contact pad region is not coplanar with a plane of an upper surface of the second region.

50. (Previously Presented) The integrated circuit device of Claim 49 wherein the plane of the second region is above the plane of the first contact pad region.

51. (Previously Presented) The integrated circuit device of claim 48 wherein the first contact pad region is configured for connection external to the device by a bond wire attached directly thereto.

52. (Previously Presented) The integrated circuit device of claim 48 wherein first contact pad region is configured for connection external to the device by a solder bump attached directly thereto.

53. (Previously Presented) The integrated circuit device of claim 48 wherein the metallization interconnect system comprises copper, and further including a barrier material located between the metallization interconnect system and the power bus in regions where the first contact pad region contacts the first interconnect feature and the second region contacts the second interconnect feature.

55. (Previously Presented) The integrated circuit device of claim 48 wherein the metallization interconnect system further comprises substantially horizontal conductive runners and substantially vertical conductive vias interconnecting overlying and underlying conductive runners.